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### IN THE CLAIMS

1. (Canceled)

2. The ~~processing system~~integrated circuit of claim 18, wherein  
the one or more cryptographic ~~items~~functions include at least one of:  
calculation of a digital signature,  
a-verification of a digital signature, and  
calculation of a cryptographic key item.

3. (Canceled)

4. The ~~processing system~~ integrated circuit of claim 18, wherein  
the link-layer access device includes a multiplication device that is configured to  
derive a second point on an elliptic curve from a first point on the elliptic curve, based on  
the one or more of the parameters from the node controller.
5. The ~~processing system~~ integrated circuit of claim 18, wherein  
the node-controller is configured to effect an exchange of a cryptographic key  
with an other processing system, and  
the one or more cryptographic items from the link-layer access device functions  
includes calculation of the cryptographic key.
6. The ~~processing system~~ integrated circuit of claim 1, wherein  
the commands from the node-controller include: a basepoint multiply command, a  
point multiply command, an EC-DSA verify command, and an EC-DSA sign command.

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (New) An integrated circuit comprising:  
a link layer access device responsive to a controller for performing  
communications between an application device and another device across a  
communications bus in accordance with a communication protocol; and  
a cryptographic accelerator responsive to said controller for performing one or  
more cryptographic functions other than encryption and decryption.

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